

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
Shunpei YAMAZAKI et al.) ATTN: New Applications
Based On: JP 2002-366158)
Filed: December 18, 2002)
For: METHOD FOR MANUFACTURING)
SEMICONDUCTOR APPARATUS, AND)
SEMICONDUCTOR APPARATUS AND)
ELECTRIC APPLIANCE)

INFORMATION DISCLOSURE STATEMENT


Commissioner for Patents
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Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing references known to Applicant and requests that these references be made of record in the above identified application. Copies of the references listed are submitted herewith in accordance with 37 C.F.R. 1.98(a).

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Respectfully submitted,



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PTO/SB/08A (08-00)

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				Application Number	
				Filing Date	
				First Named Inventor	
				Group Art Unit	
				Examiner Name	
Sheet	1	of	1	Attorney Docket Number	0756-7225

U.S. PATENT DOCUMENTS						
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FOREIGN PATENT DOCUMENTS								
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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
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		N. Hayasaka, "Recent Status of Thin Wafer Chip (die) Mounting," SEMICON JAPAN 2002, Dec. 5, 2002, pages 3-8	

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